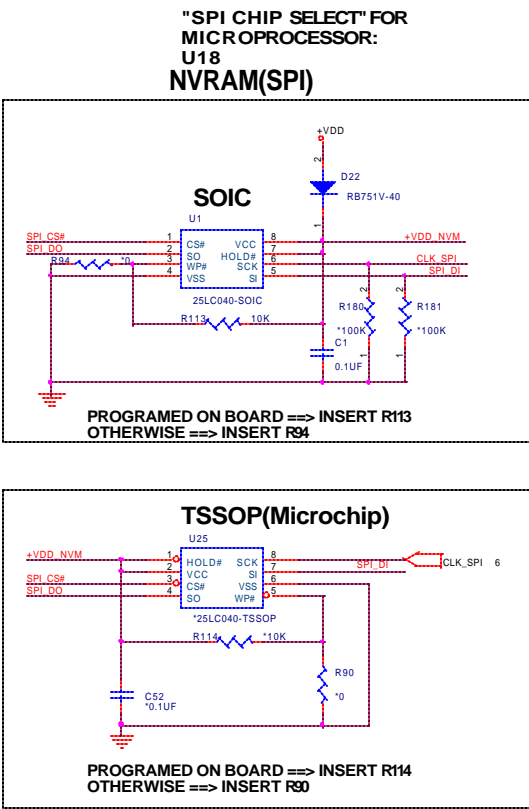
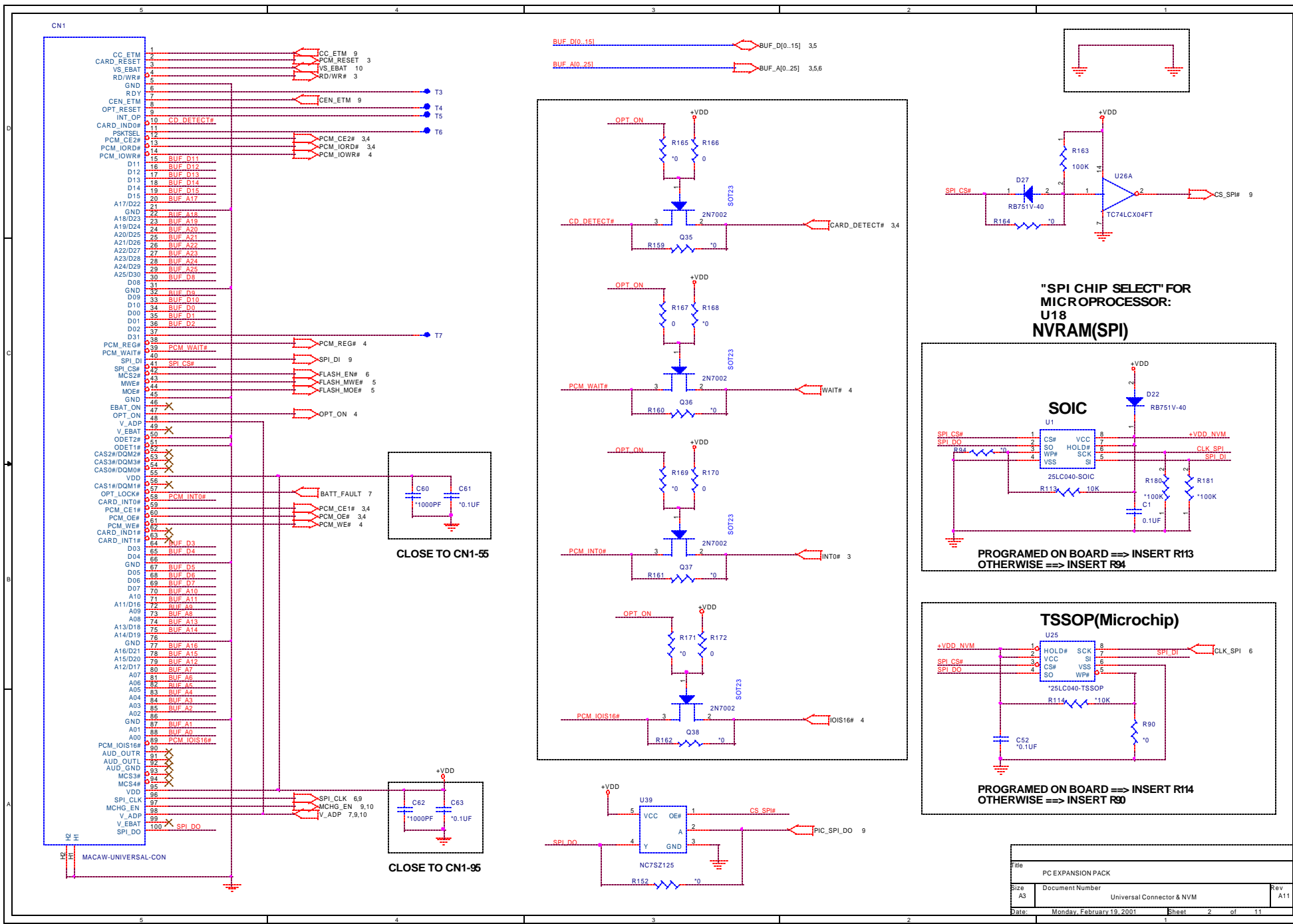
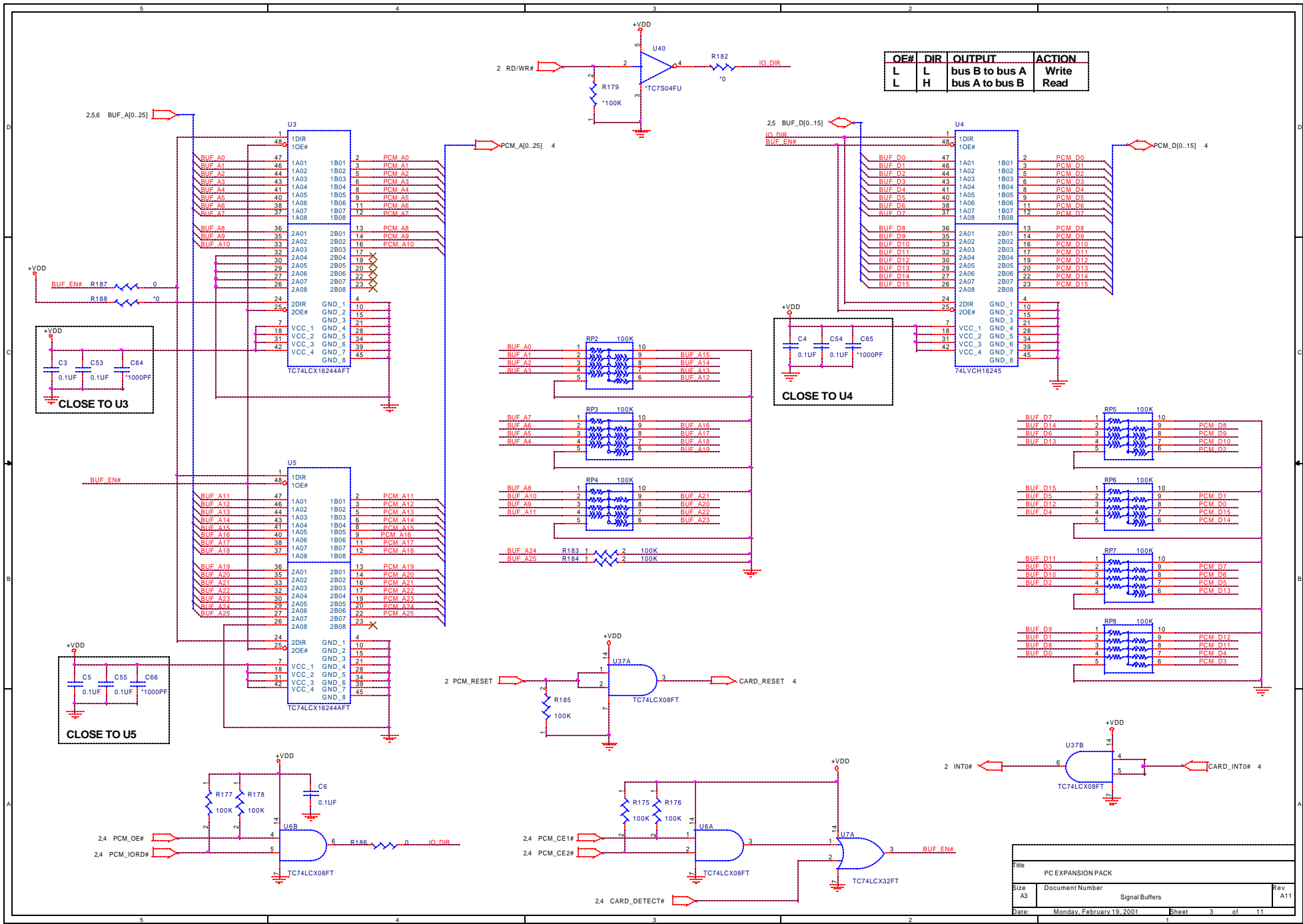
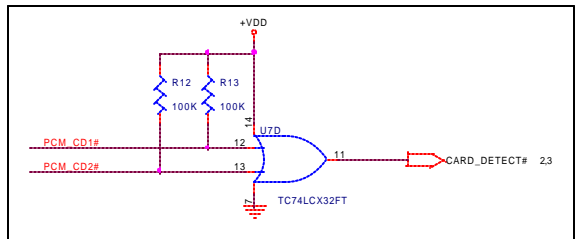
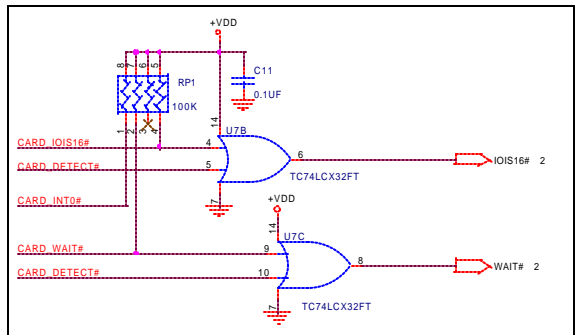
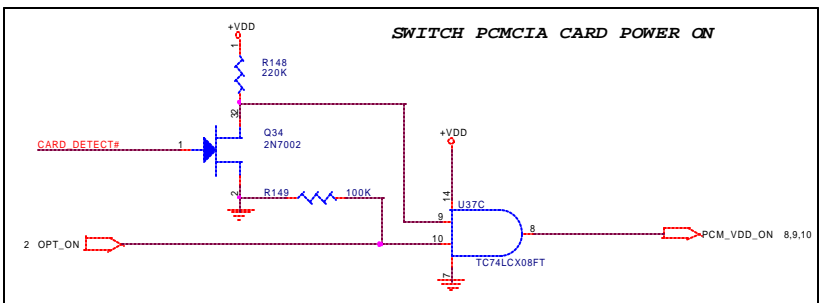
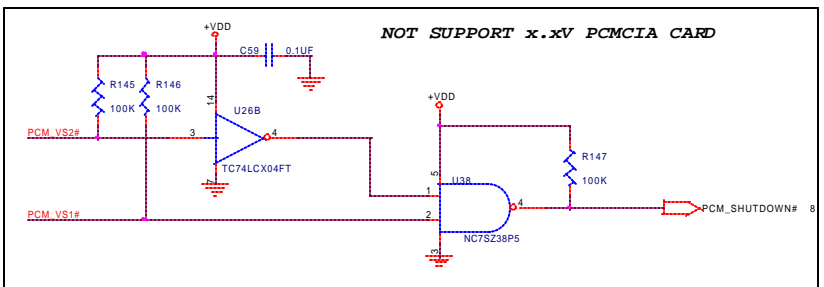
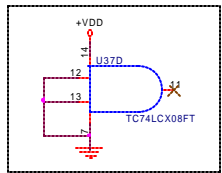
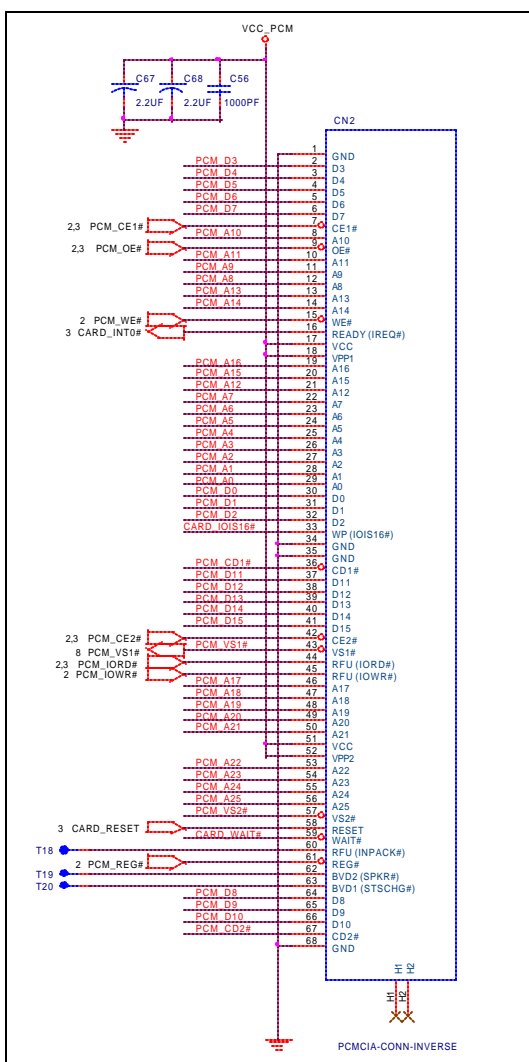


SCH01-BLOCK DIAGRAM
SCH02-UNIVERSAL CONNECTOR & NVM
SCH03-SIGNAL BUFFERS
SCH04-PCMCIA SLOT
SCH05-FLASH MEMORY
SCH06-BANK SELECTION
SCH07-POWER SWITCH
SCH08-DC TO DC
SCH09-ETM CHARGER
SCH10-AC CHARGER
SCH11-HISTORY



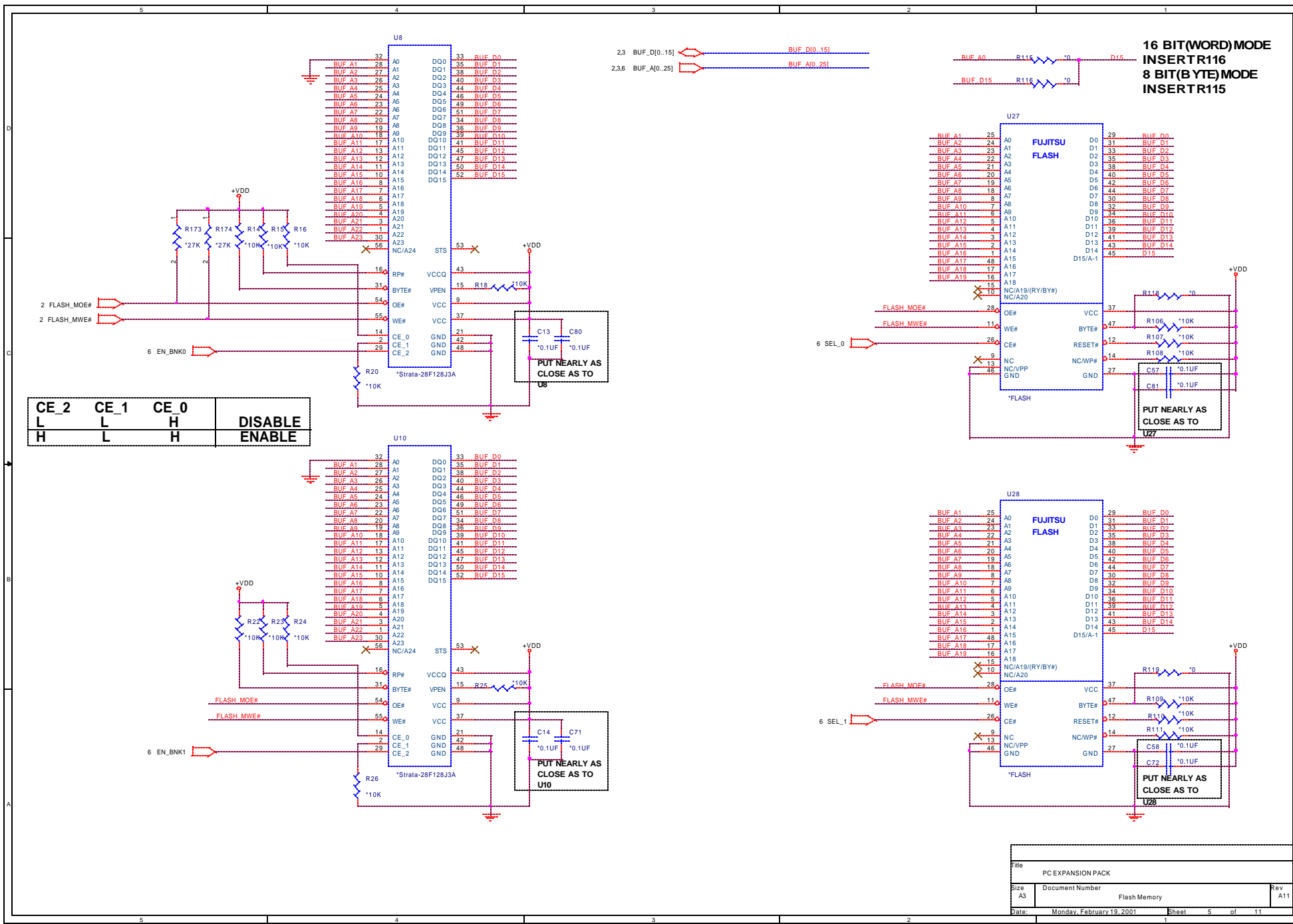


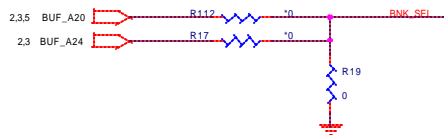
3 PCM_D[0..15] PCM_D[0..15]
 3 PCM_A[0..25] PCM_A[0..25]



DETECT IF PCMCIA INJECT OR NOT

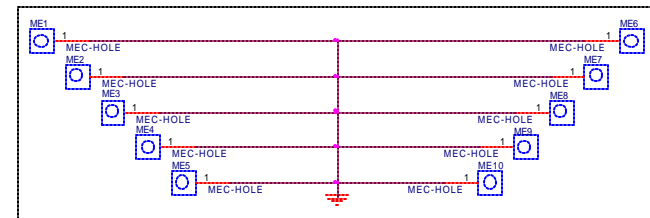
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PC EXPANSION PACK		
Size	Document Number	Rev
A3	PCMCIA Slot	A11
Date:	Monday, February 19, 2001	Sheet 4 of 11



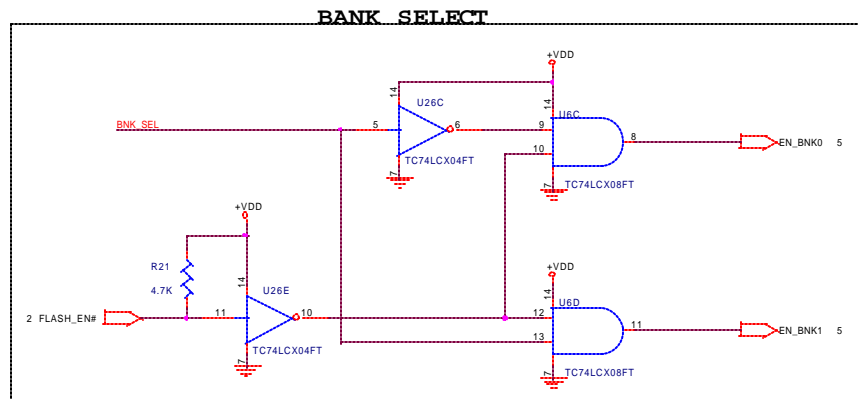


(1) For 8Mbits*2 selection
 INSERT => R19 for only one bank
 DO NOT INSERT => R17, R112
 INSERT => R112 for two banks
 DO NOT INSERT => R17, R19

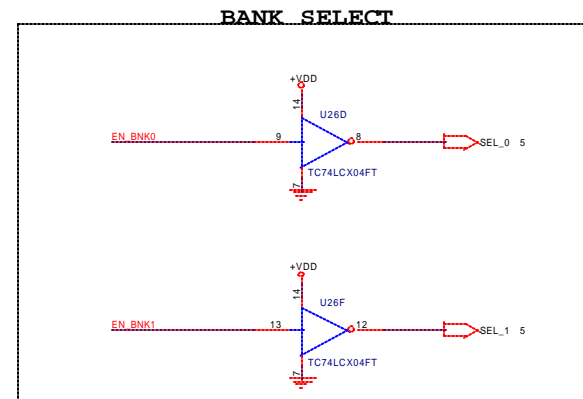
(2) For 128Mbits*2 selection
 INSERT => R19 for only one bank
 DO NOT INSERT => R17, R112
 INSERT => R17 for two banks
 DO NOT INSERT => R19, R112



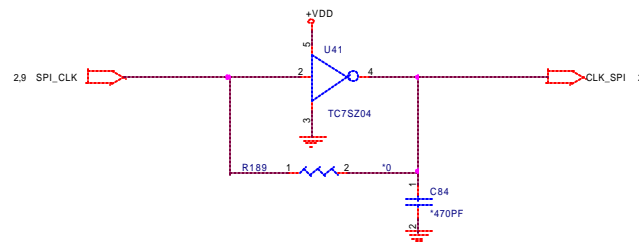
MECHANICAL-GND PADS



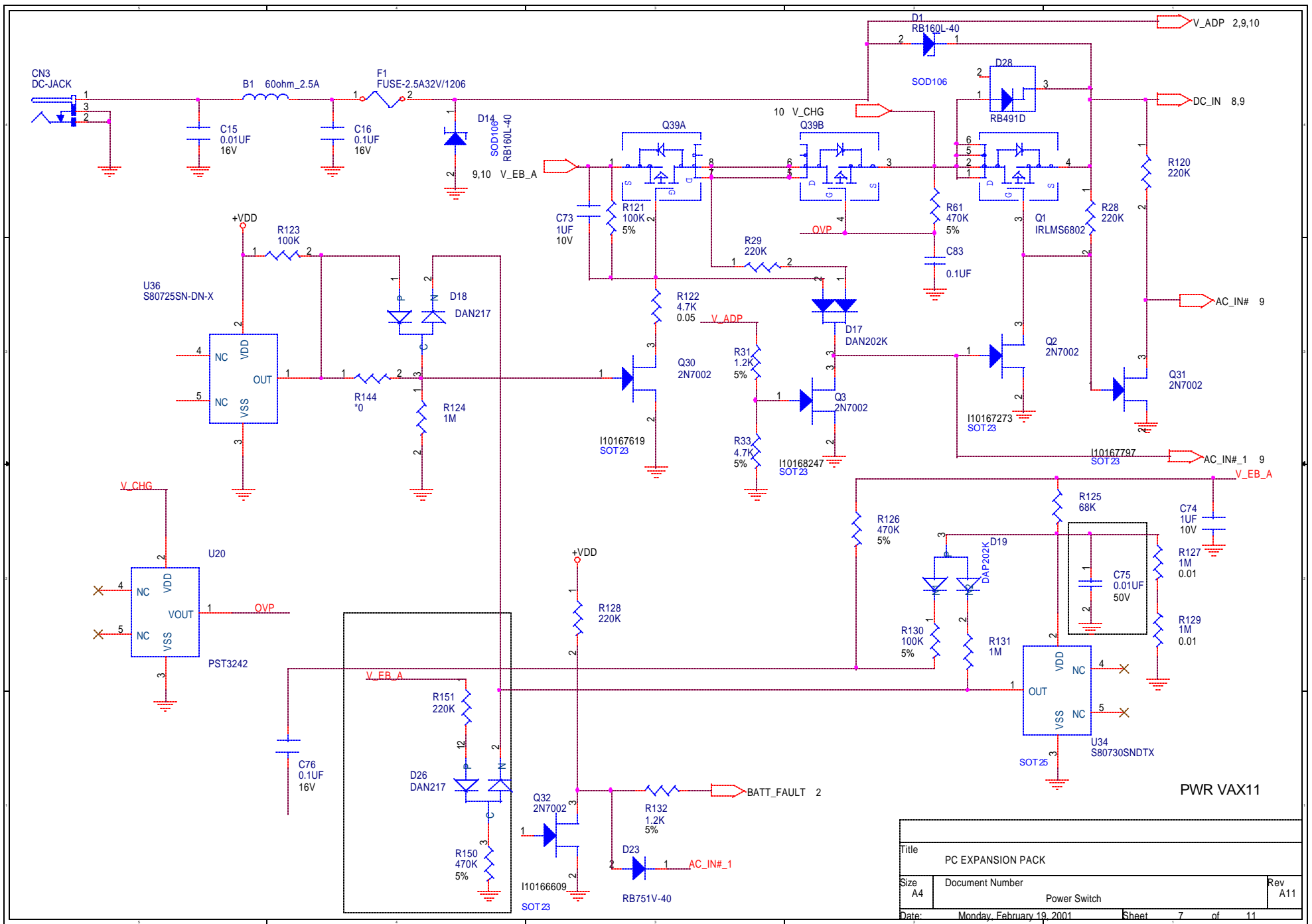
FOR 32MBytes, 2 BANKS
 STRATAFLASH

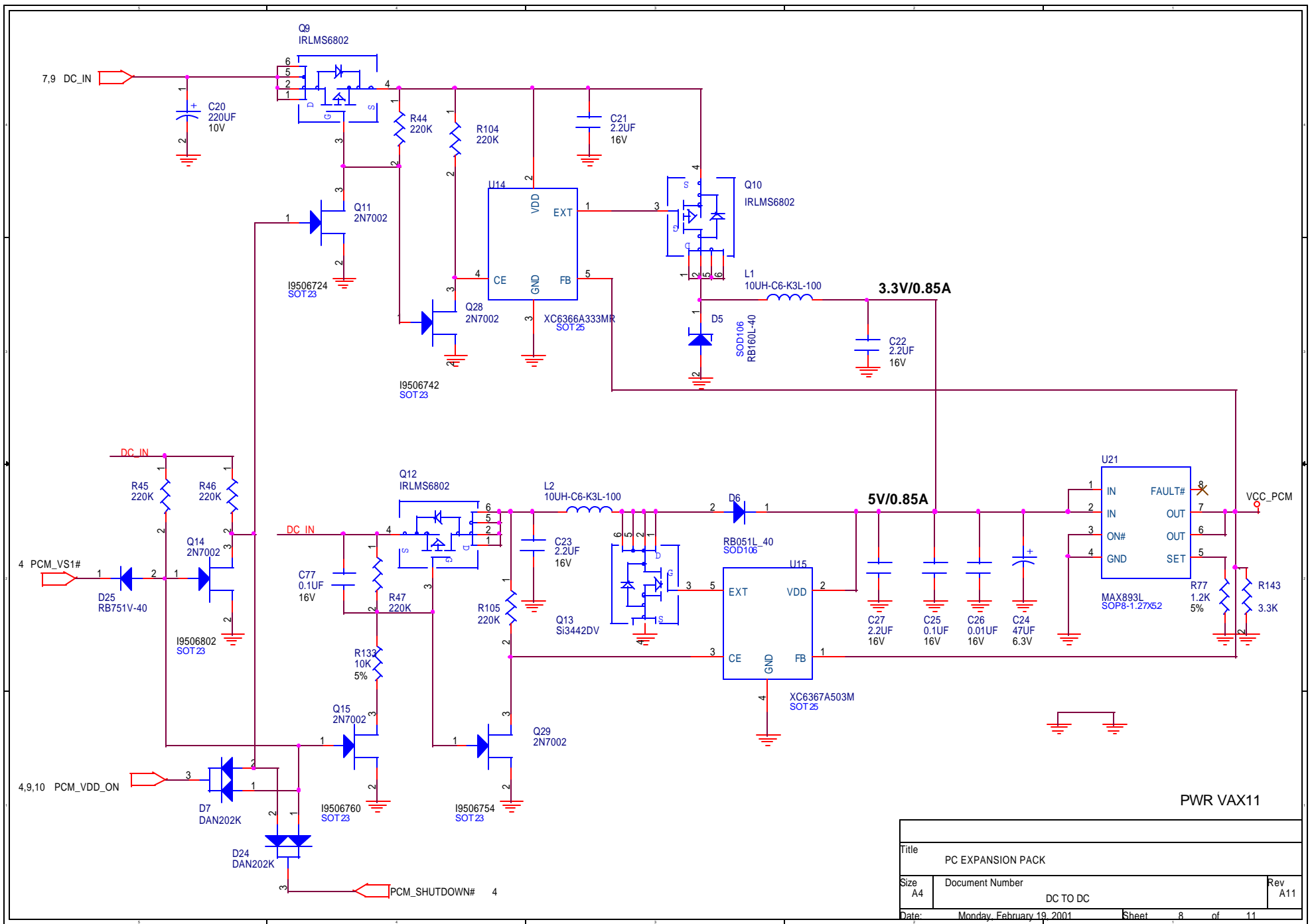


ADDITIONALLY
 FOR 2MBytes, 2 BANKS
 FLASH MEMORY



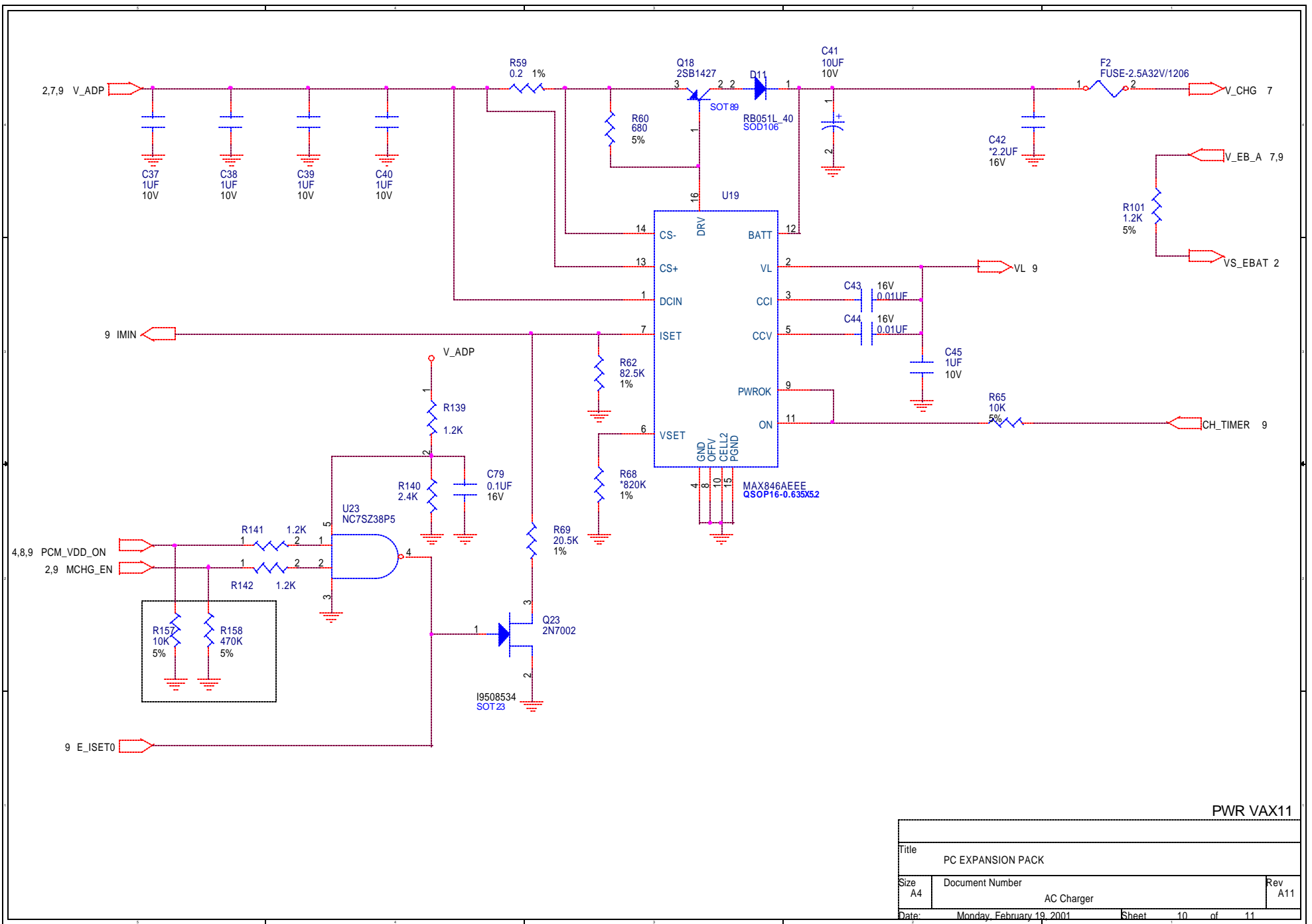
Title		
PC EXPANSION PACK		
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A3	StrataFlash Memory	A11
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Rev			
Title PC EXPANSION PACK			
Size A4	Document Number ETM Charger		Rev A11
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PWR VAX11

Title		
PC EXPANSION PACK		
Size	Document Number	Rev
A4	AC Charger	A11
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<p>2000.01.13 1. Voltage detect circuit modification for accuracy of gap between LOW1 & LOW2 2. Simplify charge current setting to be 2 steps, 0.1A & 0.5A and simplify common parts. 2000.01.28 Feature change : 128Mbits*2====>8Mbits*2 Del => U9, C12 Add => U26, U27, U28, C57, C58, C59, R106, R107, R108, R109, R110, R111, R112</p> <p>Insert => U26, U27, C57, C59, R19, R106, R107, R108, R113, R114 Not insert => U8, U10, U28, C13, C14, C58, R14, R15, R16, R17, R18, R20, R22, R23, R24, R25, R26, R109, R110, R111</p> <p>2000.01.31 Del R92, R93(0ohm U1 & U25) Add R113, R114(10kohm U1 & u25) 2000.02.11 1. CHANGE PCMCIA CONNECTOR BULK CAPACITANCE (C8, C9)-> (C67,C68) 2. RESERVE EMI/EMC BYPASS CAPACITANCE (C61,C63), (C60, C62,C64,C65,C66) 2000.02.29 1. CHANGE FLASH MEMORY ADDRESS PINS FOR 16 BIT MODE 2000.04.21 1.CHANGE LOGIC GATES TO LCX-SERIES 2.DELETE UNUSED RESISTOR-R1, R11,R91,R95-R100 3.DELETE UNLOCK SWITCH-S1 4.ADD DECOUPLING CAPACITOR 5.VERSION-A01 2000.05.02 1.ADD PCMCIA POWER LOGIC FOR CONTROLLING POWER ON/OFF 2.ADD LOGIC FOR SHUTDOWN CIRCUIT(NOT SUPPORT x.xV CARD) 2000.0505 1.ADD A BUFFER FOR ISOLATING INTERFERENCE FROM uP TO NVM 2000.05.17 1.ADD POWER LEAKAGE SOLUTION(PAGE2) 2000.05.19 1.ADD BYPASS PATH FOR OPT_ON 2000.05.25 1.ADD FLASH_MOE# & FLASH_MWE# PULL UP RESISTORS 2000.06.23 1.SOLUTION FOR SAVING POWER CONSUMPTION 2.ADD SOME RESISTORS FOR PULL UP/DOWN 3.RESERVE RDWR# CONTROL SIGNAL 2000.07.04 1.CHANGE RP1 FROM 10K TO 100K 2.CHANGE R143 FROM 10K TO 3.3K 3.REMOVE FLASH AND SOME PULL UP RESISTORS & DECOUPLING CAPACITORS 2000.07.06 1.CHANGE ADDRESS & DATA BUS PULL DOWN RESISTORS FROM 43K TO 100K(CORRECT PCN)</p>		<p>2000.09.04 1.ADD A INVERTER, CAP. AND RESISTOR TO MAKE SURE NVRAM TIMING</p> <p>2000.11.14 1. DELETE Q33,Q17 2. ADD Q39A,Q39B,D28</p>																						
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